Abstract

Read/write amplifier for a DRAM memory cell, and DRAM memory

A description is given of a DRAM memory (10) having a number of DRAM memory cells (15) which each form one or more memory cell arrays (11). Each memory cell (15) is connected to a bit line (12) and a reference bit line (13), respectively. The individual bit lines (12; 13) are furthermore connected to at least one read/write amplifier (30) according to the invention. In order that the read/write amplifier circuit (30) can perform the tasks intended for it with high evaluation reliability and speed in conjunction with the smallest possible space requirement, the invention specifies a space-saving sense amplifier scheme in which the read/write amplifier (30) has a first read/write amplifier element (40) and a second read/write amplifier element (50) separate therefrom, the individual amplifier components (41, 42, 43, 51, 54) being divided between the two read/write amplifier elements (40, 50). As a result, a single read/write amplifier (30) can be used simultaneously to evaluate a plurality of bit line pairs (16) in a single memory cell array (11).

(In this respect: Figure 3)